

<b>Notice of References Cited</b>	Application/Control No. 09/810,518	Applicant(s)/Patent Under Reexamination YONEZAWA ET AL.	
	Examiner Russell Frejd	Art Unit 2128	Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
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	B	US-6,278,964	08-2001	Fang et al.	703/19
	C	US-			
	D	US-			
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	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
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**NON-PATENT DOCUMENTS**

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	U	YONEZAWA et al., H. Ratio Based Hot-Carrier Degradation Modeling for Aged Timing Simulation of Millions of Transistors Digital Circuits, Electron Devices Meeting, IEDM '98, IEEE, December 1998, pages 93-96.
	V	CHANG et al., C-W. Layout-Driven Hot-Carrier Degradation Minimization Using Logic Restructuring Techniques, Proceedings of the 38th Conference on Design Automation, June 2001, pages 97-102.
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\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.